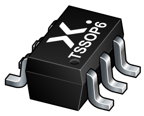

PMP5501Y-Q

45 V, 100 mA PNP/PNP matched double transistor

12 September 2025 — Product data sheet

1. General description

PNP/PNP matched double transistor in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

PNP/PNP hFE1/hFE2 0.98 complement: PMP5201Y-Q

NPN/NPN complement: PMP4501Y-Q

2. Features and benefits

- Current gain matching
- Base-emitter voltage matching
- Application-optimized pinout
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Current mirror
- Differential amplifier

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	-45	V
I_C	collector current			-	-	-100	mA
h_{FE}	DC current gain	V_{CE} = -5 V; I_C = -2 mA; T_{amb} = 25 °C		200	290	450	
Per device							
h_{FE1}/h_{FE2}	DC current gain matching	V_{CE} = -5 V; I_C = -2 mA; T_{amb} = 25 °C		0.95	1	-	
$V_{BE1}-V_{BE2}$	base-emitter voltage matching			-	-	2	mV

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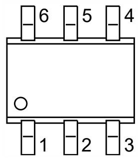
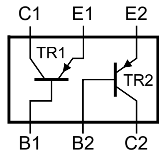
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B1	base TR1	 TSSOP6 (SOT363)	
2	B2	base TR2		
3	C2	collector TR2		
4	E2	emitter TR2		
5	E1	emitter TR1		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMP5501Y-Q	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMP5501Y-Q	S6%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	-50	V
V_{CEO}	collector-emitter voltage	open base		-	-45	V
V_{EBO}	emitter-base voltage	open collector		-	-5	V
I_C	collector current			-	-100	mA
I_{CM}	peak collector current	single pulse; $t_p \leq$ 1 ms		-	-200	mA
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1] [2]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1] [2]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Reflow soldering is the only recommended soldering method.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	416	K/W

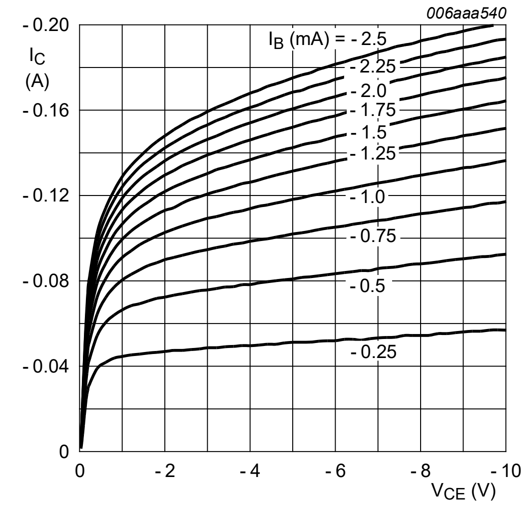
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Reflow soldering is the only recommended soldering method.

10. Characteristics

Table 7. Characteristics

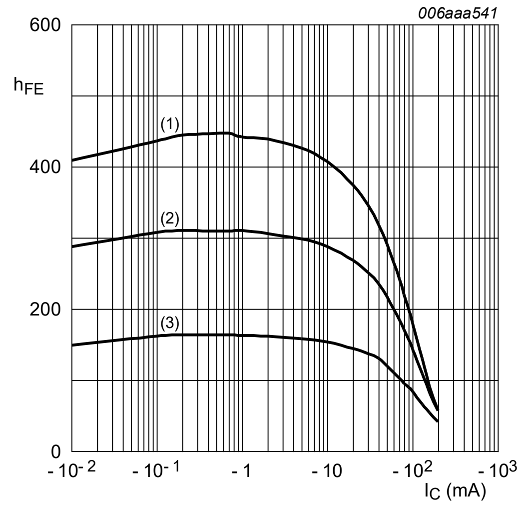
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = -30 V; I_E = 0 A; T_{amb} = 25 °C		-	-	-15	nA
		V_{CB} = -30 V; I_E = 0 A; T_j = 150 °C		-	-	-5	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	-100	nA
h_{FE}	DC current gain	V_{CE} = -5 V; I_C = -10 μA; T_{amb} = 25 °C		-	250	-	
		V_{CE} = -5 V; I_C = -2 mA; T_{amb} = 25 °C		200	290	450	
V_{CEsat}	collector-emitter saturation voltage	I_C = -10 mA; I_B = -0.5 mA; T_{amb} = 25 °C		-	-50	-200	mV
		I_C = -100 mA; I_B = -5 mA; T_{amb} = 25 °C		-	-200	-400	mV
V_{BEsat}	base-emitter saturation voltage	I_C = -10 mA; I_B = -0.5 mA; T_{amb} = 25 °C	[1]	-	-760	-	mV
		I_C = -100 mA; I_B = -5 mA; T_{amb} = 25 °C	[1]	-	-920	-	mV
V_{BE}	base-emitter voltage	V_{CE} = -5 V; I_C = -2 mA; T_{amb} = 25 °C	[2]	-600	-650	-700	mV
		V_{CE} = -5 V; I_C = -10 mA	[2]	-	-	-760	mV
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.2	pF
C_e	emitter capacitance	V_{EB} = -0.5 V; I_C = 0 A; i_c = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	10	-	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -10 mA; f = 100 MHz; T_{amb} = 25 °C		100	175	-	MHz
NF	noise figure	V_{CE} = -5 V; I_C = -0.2 mA; R_S = 2 kΩ; f = 10 Hz to 15.7 kHz; T_{amb} = 25 °C		-	1.6	-	dB
		V_{CE} = -5 V; I_C = -0.2 mA; R_S = 2 kΩ; f = 1 kHz; B = 200 Hz		-	3.1	-	dB
Per device							
h_{FE1}/h_{FE2}	DC current gain matching	V_{CE} = -5 V; I_C = -2 mA; T_{amb} = 25 °C		0.95	1	-	
$V_{BE1}-V_{BE2}$	base-emitter voltage matching			-	-	2	mV

[1] V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.
[2] V_{BE} decreases by about 2 mV/K with increasing temperature.



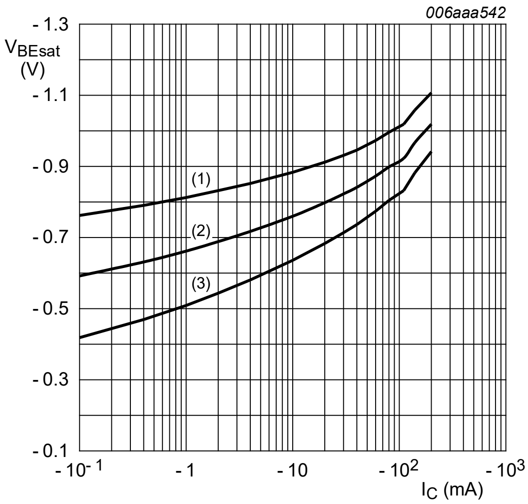
T_{amb} = 25 °C

Fig. 1. Per transistor: Collector current as a function of collector-emitter voltage; typical values



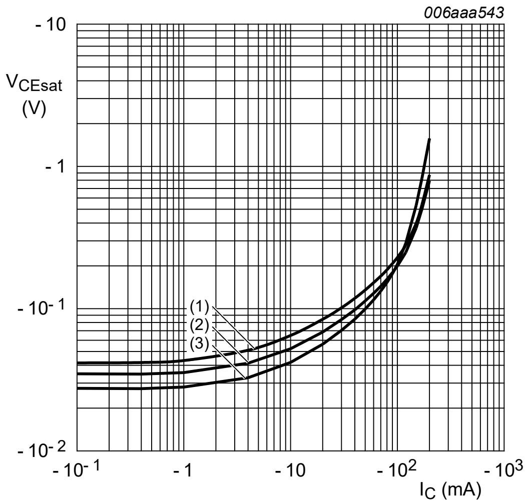
V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 2. Per transistor: DC current gain as a function of collector current; typical values



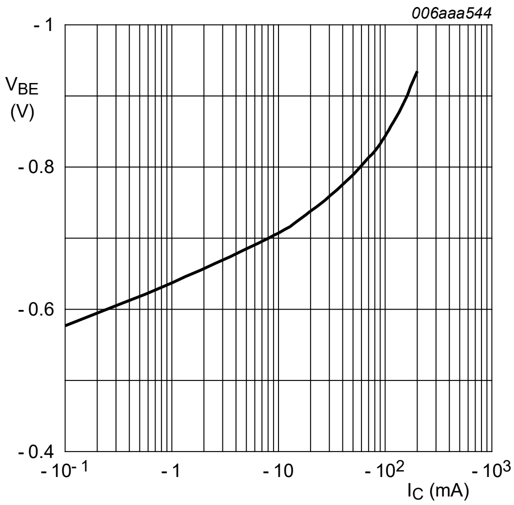
I_C/I_B = 20
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 3. Per transistor: Base-emitter saturation voltage as a function of collector current; typical values



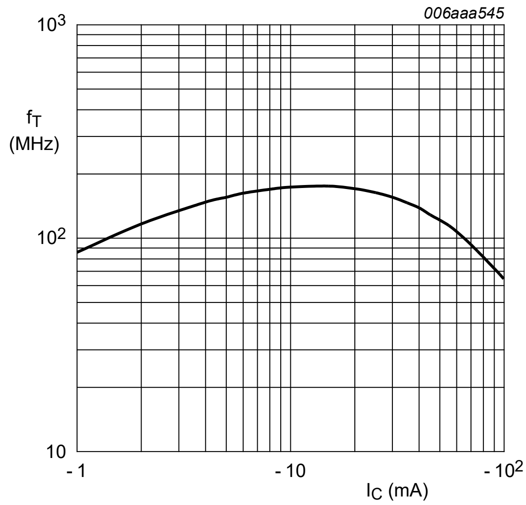
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 4. Per transistor: Collector-emitter saturation voltage as a function of collector current; typical values



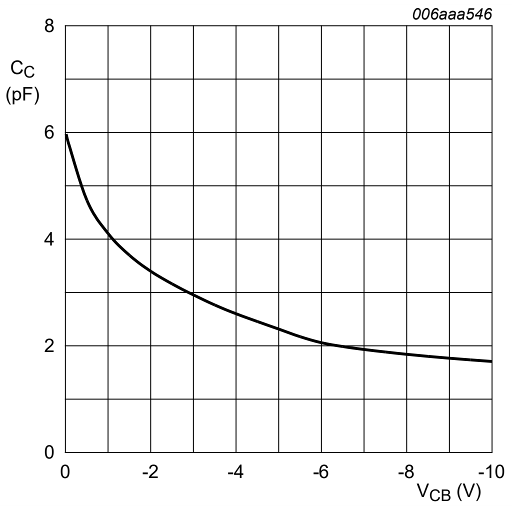
V_{CE} = -5 V; T_{amb} = 25 °C

Fig. 5. Per transistor: Base-emitter voltage as a function of collector current; typical values



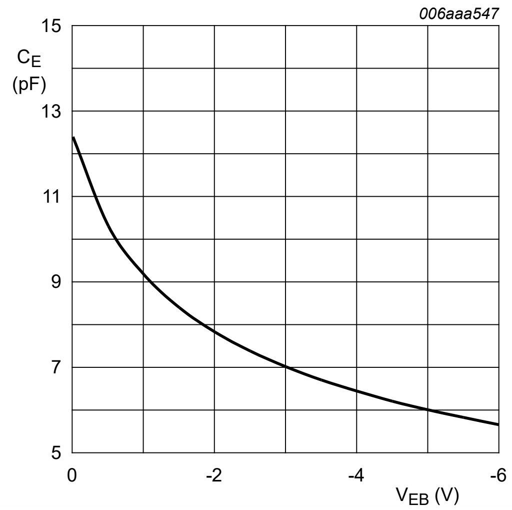
V_{CE} = -5 V; T_{amb} = 25 °C

Fig. 6. Per transistor: Transition frequency as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 7. Per transistor: Collector capacitance as a function of collector-base voltage; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 8. Emitter capacitance as a function of emitter-base voltage; typical values

11. Application information

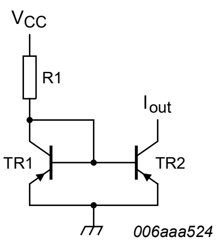


Fig. 9. Current mirror

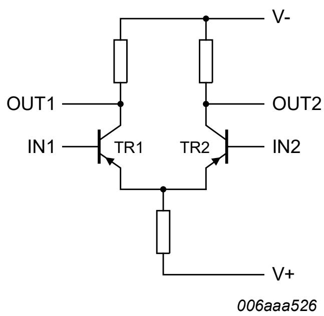


Fig. 10. Differential amplifier

12. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard*Q101 -Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

13. Package outline

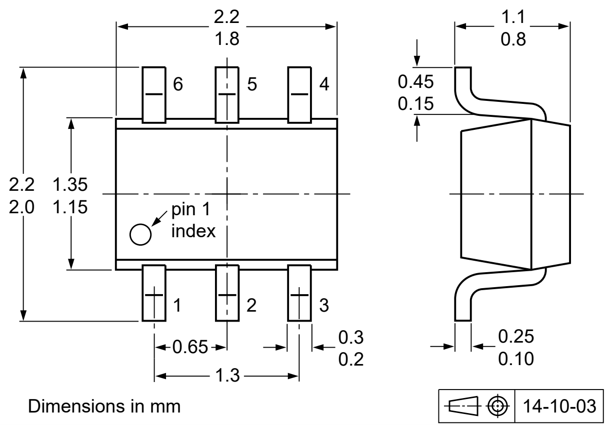


Fig. 11. Package outline TSSOP6 (SOT363)

14. Soldering

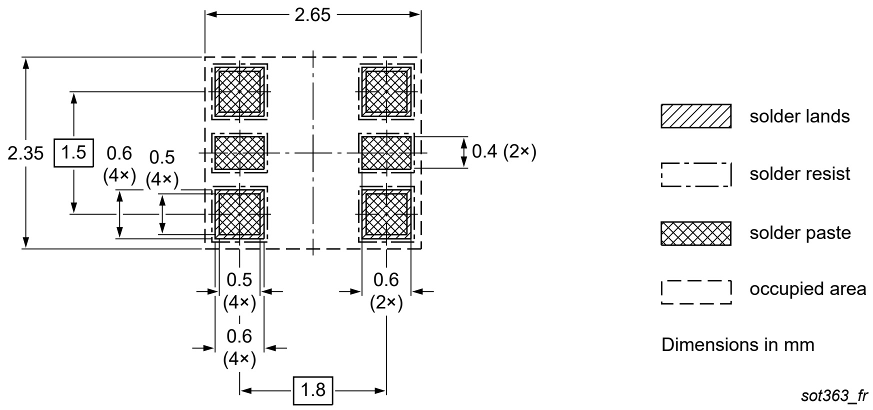


Fig. 12. Reflow soldering footprint for TSSOP6 (SOT363)

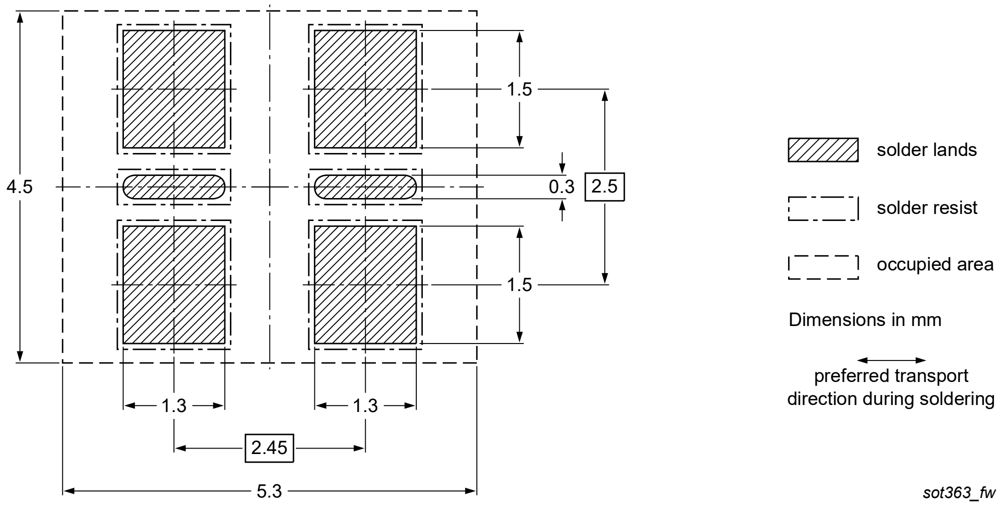


Fig. 13. Wave soldering footprint for TSSOP6 (SOT363)

15. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMP5501Y-Q v.1	20250912	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 12 September 2025